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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,366	09/19/2000	Douglas O. Powell	EN9-99-026	5058

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Burton A Amernick Esquire
Pollock Vande Sande & Amernick RLLP
P O Box 19088
Washington, DC 20036-3425

EXAMINER	
COMPTON, ERIC B	
ART UNIT	**PAPER NUMBER**
3726	

DATE MAILED: 10/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/665,366	POWELL, DOUGLAS O.	
	Examiner	Art Unit	
	Eric B. Compton	3726	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 10 September 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 4 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☒ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *see attached*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-80*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. The declaration filed on September 10, 2004 under 37 CFR 1.131 is sufficient to overcome the McCormack (US Pat. 6,054,761) reference.

THE FOLLOWING IS AN EXPLANATION OF HOW THE CLAIMS WOULD BE REJECTED:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 7-10, 12-14, 16-18, 20-21, 37-42, 45-48, 51- 53, 64-68, and 79-80, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,744,758 to Takenouchi et al in view of U.S. Patent 5,837,119 to Kang et al ("Kang").

Takenouchi et al disclose a multi-layered electronic structure and a method for making said structure (see Figures 7(a)-7(e), 8, & 9), comprising the steps of:

a. Providing a plurality of sub-composites (12) comprising: providing a layer of dielectric material (14,16) having a top and bottom;

b. providing a layer of electrically conducting material (13) on one of the top surface of the dielectric layer;

c. forming at least one passage (18) through the dielectric layer;

d. depositing electrically conducting material (32, 34) in at least one of the at least one passage through the dielectric layer;

e. removing portions of the layer of electrically conducting material to define a pattern of circuitry (see Figures 7(d) and 7(e));

f. stacking a plurality of sub-composites (Figure 9);

g. aligning the plurality of sub-composites (it is inherent that the structures are aligned);

h. joining the plurality of sub-composites such that the electrically conducting material in at least one on the at least one the blind vias makes electrically contact by forming a metallurgical bond (see col. 10, lines 65-67) to the conductive pattern (by heat press, col 11, lines 63-65); and

i. filling the spaces between adjacent sub-composites with electrically insulating material (via heat pressing, see Figure 8).

However, Takenouchi et al do not disclose that conductive paste forms a metallurgical bond.

Kang discloses a conductive paste of the type disclosed by both Takenouchi and Applicant "for forming electroconductive connections between electroconductive members and methods of use in electronic applications." Col. 1, lines 10-13; *see also* Figure 2B. The reference further discloses

> According to an embodiment of the present invention, ***an electrically conductive paste (ECP) material is disclosed***, which consists of copper powder coated with a thin layer of low melting point, Pb-free metals, such as Sn, In, Bi, Sb and their alloys, mixed with an environmentally-safe fluxing agent, and dispersed in the matrix of thermoplastic or thermosetting polymers. The

microstructure of the ECP containing Sn-coated Cu powder is shown in its cross-section view in FIG. 3.

In one particular embodiment, we disclose a new electrically conductive paste material consisting of indium-coated copper powder, polyimide-siloxane, solvent (NMP), no clean flux, and carboxylic acid/surfactant. The indium-coated copper powder is produced by a sequential electrodeposition of copper dendrite powder on a dummy substrate, followed by another electrodeposition of indium on the copper dendrite powder. The copper dendrite powder can be replaced by other dendritic powders such as nickel, cobalt, chromium, palladium, platinum, and others. The indium can be replaced by other metals such as Sn, Zn, Pb, Bi and Sb or their alloys. Because the dendritic powder has a large aspect ratio, it has an advantage of better electrical and/or thermal conduction characteristics in comparison to the spherical powder. ***A joining operation can be performed near the melting point of In, 157.degree. C., where a metallurgical bonding of In-to-In or In-to-Au or In-to-Cu is accomplished at the dendritic particle-to-particle as well as dendritic particle-to-substrate pad interfaces***. Since indium metal and alloys have an excellent wetability on the metals that are hard to solder to, such as aluminum, titanium, molybdenum, or tungsten, the present invention material can be used for joining of liquid crystal display devices. The joining process can be either solid-state or liquid-solid reaction. The polymer curing process can be combined with the joining process depending on the paste formulation. ***Because of the metallurgical bonding and the high conductivity copper core, a higher electrical conductivity is expected with the joints made of the new paste material than with those of the silver-epoxy material. The metallurgical bonds also provide stable electrical conductivity of the new joints upon thermal exposure and cycling. It is also expected to have a higher joint strength from the combined effect of the metallurgical and adhesive bonds.***

Col. 4, line 35 – Col. 5, line 9 (emphasis added).

Regarding claims 1, 46, and 68, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the multi-layered electronic structure by the method of Takenouchi et al using a conductive paste capable of forming metallurgical bonds, in light of the teachings of Kang, in order to provide a more reliable bonds resistant to high thermal cycling.

Regarding claims 66 and 67, an electronic package, formed by the method above is shown and described. Furthermore, it is inherent that such structures are used for mounting electrical components.

Regarding claims 2-3, and 47-48, Takenouchi al disclose that the dielectric layer (16) may be polyimide (col 6, line 4)

Regarding claim 7, it is inherent in Takenouchi et al that the conducting material may be solderable (col 9, lines 38-40).

Regarding claims 8-9, 14, and 51-52, Takenouchi et al disclose that the conducting material is copper foil (col 10, line 30).

Regarding claims 10 and 12, Takenouchi et al disclose that the conducting material may be electroplated (col 10, line 38).

Regarding claim 13, this step is inherently accomplished in Takenouchi et al.

Regarding claims 16 and 45, Takenouchi et al disclose that the conducting material is patterned with a resist, which is a protective cover.

Regarding claim 17, Takenouchi et al disclose that the passages may be formed by laser (col 10, line 33).

Regarding claim 18, see Figure 7(e) of Takenouchi et al, wherein the conducting material deposited in a passage does not extend beyond the opening of the passage.

Regarding claims 20-21, and 53, Takenouchi et al disclose that the conducting material is a metal deposited in the passages in by platting (col 10, line 5).

Regarding claims 37-41, Takenouchi et al discloses bonding via pressure in a vacuum under inert atmosphere (see col, 10, lines 55-60).

Regarding claims 42, 64, and 65, Takenouchi et al inherently disclose that the structures are filled with a thermoset plastic (16, see col 12, lines 3-5).

Regarding claims 79-80, Kang discloses that the conductive paste has metal particles, which will inherently fuse when melted.

4. Claims 4-6, 11, 15, 19, 24-33, 35-36, 49-50, 54- 58, and 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al/Kang in view of US Patent 4,915,983 to Lake et al.

Takenouchi et al/ Kang disclose the invention cited above. However, they do not disclose the particulars of the invention as claimed by Applicant.

Lake et al disclose a multi-layered electronic structure and a method for making said structure (see Figure 8) very similar in structure to both Takenouchi et al and Applicant's inventions. Many of the particulars not disclosed by Takenouchi et al are disclosed Lake et al, which are apparently all in the art of forming interconnects.

Regarding claims 4-6, 11, 15, 19, 24-33, 35-36, 49-50, 54- 58, and 60-63, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the sub-composites of Takenouchi et al/Kang using the various interconnect forming techniques well-known in the art, in light of the teachings of Lake et al, in order to take advantage of well-known interconnect forming technology, thus saving capital costs on retooling production lines for new product runs.

Regarding claims 4 and 49, Official Notice is taken that liquid crystal polymer film is well known in the circuit board arts and a skilled artisan would have found it obvious at time of invention to use such in the method of Takenouchi et al/Kang.

Regarding claims 5, and 50, Lake et al disclose that the dielectric (50) may be polyimide (col 9, line 33) and/or include a mesh or screen of glass (col 10, lines 37-38).

Regarding claim 15, Lake et al disclose that the dielectric material is applied to the foil using a press roll (col 9, line 15).

Regarding claim 6, see Figure 8, step 1 of Lake et al.

Regarding claim 11, Official Notice is taken that applying a coating by physical vapor deposition to a substrate comprising vacuum evaporation or sputtering is well known in the art and a skilled artisan would have found it obvious at time of invention to use such in the method of Takenouchi et al.

Regarding claim 19, see Figure 8, step 5, or Lake et al.

Regarding claims 24-26, 28, 29, 30, 31, 33, 54, 55, and 56, Lake et al disclose a layer of tin lead alloy may be applied over the copper foil by a continuous electroplating process (col 9, lines 57-59).

Regarding claims 27 and 57, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provide a cap having a thickness of 0.0001 to .0004 inch, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 32, Takenouchi et al disclose that the circuitry is formed by resist patterning (col 10, lines 48-50).

Regarding claims 35, 60-62, Official Notice is taken that aligning structure such as providing holes in the laminate layers and a jig having corresponding aligning pins

and indicia (registration marks) are well known in the art. Applicant, also alludes to the fact such structures are known, referring to slots and pins as standard alignment means (page 34, lines 2-3).

Regarding Claims 36 and 63, Lake et al disclose that the layers will be soldered coated (col 9, line 39).

Regarding claim 58, Official Notice is taken that coating a substrate with oxides (e.g. tin oxide) are known in the art to roughen the surface for subsequent bonding and a skilled artisan would have found it obvious at time of invention to apply a coating for such purpose.

5. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al/Kang in view of US Patent 3,601,523 to Arndt.

Takenouchi et al/Kang disclose the invention cited above. However, they do not disclose that the conducting material provided in the passage is a conducting paste.

Arndt discloses a method for filling a passageway with a conducting paste in order to conductively contact the circuitry from one side of a dielectric to another.

Regarding claim 22, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a conducting paste in the passage of Takenouchi et al/Kang, in light of the teachings of Arndt, in order to provide a more low resistant connection than by platting (see col 1, lines 60+).

Regarding claim 23, Arndt uses a squeegee (20) to apply the conducting paste.

6. Claims 34 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al/Kang in view of US Patent 4,921,157 to Dishon et al.

Takenouchi et al/Kang disclose the invention cited above. However, they do not disclose treating the dielectric layer and patterned circuitry with fluorine-containing plasma.

Dishon et al/Kang disclose a method for treating a circuit board with exposed soldering. The surfaces are treated with a fluorine-containing plasma in order to remove oxides and provide a more efficient solder joint.

Regarding claims 34 and 59, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have treated the structure of Takenouchi et al/Kang with fluorine-containing plasma, in light of the teachings of Dishon et al, in order to remove surface oxides from the solder contacts.

7. Claims 37-44 and 69-78 rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al/Kang in view of US Patent 5,635,010 to Pepe et al.

Takenouchi et al/Kang disclose the invention cited above. The reference relies on pressure and heat to bond the structures. However, it does not specifically disclose providing filling the spacing between adjacent structures with a liquid, which is transformed into a solid.

Pepe et al disclose a method for bonding layers to form a laminate (see Figures 9-12). A dielectric adhesive, preferably a polyimide, applied as a liquid is provide on the to close voids and help bond substrates together. "The preferred polyimide exhibits sufficient viscous flow at the initial temperature and pressure conditions such that it fills all voids between adjacent chips and excess adhesive extrudes from the chip stack to achieve minimal thickness of the adhesive layer" (col 7, lines 58-63).

Regarding claims 37 and 69, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided a liquid insulator to bond the structures of Takenouchi et al/Kang, in light of the teachings of Pepe et al, in order to fill the voids between the structures.

Regarding claims 37-44, and 76-78, see col 8, lines 49-64 of Pepe et al regarding bonding with pressure in a vacuum with an inert atmosphere.

Regarding claims 70-71, the liquid may include epoxy, an organic resin.

Regarding claims 73-74, Official Notice is taken that inorganic filler and cross-linking is the art to provide structures of added strength and that a skilled artisan would have found it obvious at the time of invention to have provided either for such purpose.

Regarding claim 74, it is inherent that the liquid resin is moved by capillary action.

Regarding claim 75, the liquid resin is placed on the top periphery of the structures.

Remarks

8. The after final amendment dated September 10, 2004 has been entered. The amendment overcomes the previous indicated 112, first paragraph rejections.

9. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection above.

10. As indicated above, the declaration is sufficient for overcoming the rejections based on the teachings of McCormack. McCormack was relied on as a secondary

teaching that the conductive paste forms a metallurgical bond. The primary reference, Takenouchi, discloses a method forming a multi-layered electronic structure using a conductive paste. However, the reference does not explicitly disclose the metallurgical bonding.

11. U.S. Pat. 5,837,119 to Kang et al ("Kang") disclose a conductive paste of the type disclosed by both Takenouchi and Applicant "for forming electroconductive connections between electroconductive members and methods of use in electronic applications." Col. 1, lines 10-13; *see also* Figure 2B. The reference further discloses

> According to an embodiment of the present invention, ***an electrically conductive paste (ECP) material is disclosed***, which consists of copper powder coated with a thin layer of low melting point, Pb-free metals, such as Sn, In, Bi, Sb and their alloys, mixed with an environmentally-safe fluxing agent, and dispersed in the matrix of thermoplastic or thermosetting polymers. The microstructure of the ECP containing Sn-coated Cu powder is shown in its cross-section view in FIG. 3.
>
> In one particular embodiment, we disclose a new electrically conductive paste material consisting of indium-coated copper powder, polyimide-siloxane, solvent (NMP), no clean flux, and carboxylic acid/surfactant. The indium-coated copper powder is produced by a sequential electrodeposition of copper dendrite powder on a dummy substrate, followed by another electrodeposition of indium on the copper dendrite powder. The copper dendrite powder can be replaced by other dendritic powders such as nickel, cobalt, chromium, palladium, platinum, and others. The indium can be replaced by other metals such as Sn, Zn, Pb, Bi and Sb or their alloys. Because the dendritic powder has a large aspect ratio, it has an advantage of better electrical and/or thermal conduction characteristics in comparison to the spherical powder. ***A joining operation can be performed near the melting point of In, 157.degree. C., where a metallurgical bonding of In-to-In or In-to-Au or In-to-Cu is accomplished at the dendritic particle-to-particle as well as dendritic particle-to-substrate pad interfaces***. Since indium metal and alloys have an excellent wetability on the metals that are hard to solder to, such as aluminum, titanium, molybdenum, or tungsten, the present invention material can be used for joining of liquid crystal display devices. The joining process can be either solid-state or liquid-solid reaction. The polymer curing process can be combined with the joining process depending on the paste formulation. ***Because of the metallurgical bonding and the high conductivity***

> ***copper core, a higher electrical conductivity is expected with the joints made of the new paste material than with those of the silver-epoxy material. The metallurgical bonds also provide stable electrical conductivity of the new joints upon thermal exposure and cycling. It is also expected to have a higher joint strength from the combined effect of the metallurgical and adhesive bonds.***

Col. 4, line 35 – Col. 5, line 9 (emphasis added). Thus, the use of a conductive paste having conductive particles forming a metallurgical bond between adjacent particles and between the particles and substrate was known prior to Applicant filing of the application, September 19, 2000, and the date sworn behind in the declaration, based on the IBM disclosure having a date of September 9, 1998.

12. It is noted that the publication date of Kang (same assignee IBM) is November 17, 1998, filed August 9, 1996, which is more than one (1) year prior to the filing date of the instant application, filed September 19, 2000. Thus, Kang constitutes a 102(b) reference, which cannot be overcome by the 37 CFR 1.131 declaration.

13. The finality of the action is maintained since Applicant's amendment prompted the new grounds of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Compton whose telephone number is (703) 305-0240. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter B. Vo can be reached on (703) 308-1789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Compton
Patent Examiner